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Doctoral school: EDMI (Bordeaux)
Thesis date: 14/10/2020 – 14/10/2023
Financing: CTBU
CONTEXT & MOTIVATIONS

DNEURO, DNN IP for FPGA ¹

Xilinx Virtex™ 5 Rapid ASIC/SOC Prototyping System ²

Deep-Learning and HPC to Boost Biomedical Applications for Health ³

1: https://www.cea.fr/cea-tech/leti/Documents/d%C3%A9monstrateurs/Flyer_DNEURO.pdf
2: http://www.hitechglobal.com/boards/v5_multi_lx330.htm
3: https://deephealth-project.eu
• Performance is dominated by the timing critical path (logical depth and TDM)
• (Hyper)-graph partitioning is NP-Hard $^1$ $^2$

![Result for 3elt graph with SCOTCH $^3$](image1)

![Partitioning of BRACKET into 8 parts with SCOTCH $^3$](image2)

• There exist some tools to cut an hypergraph: hMetis $^4$, PaToH $^5$, KaHyPar $^6$, etc.

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Min-cut does not solve the path delay-based minimization.

Min-cut = 1, Min-path-delay = 2 + penalty

Min-cut = 3, Min-path-delay = 1 + penalty
STATE OF THE ART & RESEARCH TOPICS

- Certain work handle the problem

1. Jun 'ichiro MINAMI, Tetsushi KOIDE, Shin'ichi WAKXBAYASHI, A Circuit Partitioning Algorithm under Path Delay Constraints (Hiroshima University), IEEE. APCCAS 1998
3. Cristinel Ababei, Navaratnasothie Selvakumaran, Kia Bazargan, George Karypis, Multi-objective Circuit Partitioning for Cutsizes and Path-Based Delay Minimization (University of Minnesota), ICCAD 2002
4. Sin-Hong Liou, Sean Liu, Richard Sun and Hung-Ming Chen Timing Driven Partition for Multi-FPGA Systems with TDM Awareness (University Hsinchu and Synopsys), ISPD 2020

(a) Placement result without penalty.  (b) Placement result with penalty.
• Model
  • Netlist to a directed hypergraph
  • Vertex has vector of weights (capacitance constraints)
  • Hyperedges has weighted pins and a main weight (delay constraints)
  • Path model \((v_0, e_0, \ldots, e_{n-1}, v_n)\) (critical path constraint)

• Different ways to model the path cost
• Operational concerns:
  • Improvement of the model
  • Implementation of a prototype in Python 3.9

• Personal:
  • Current status:
    • Covid lockdown (I never saw my thesis director 😞)
    • Yet teaching at University of Bordeaux (Algorithmique des tableaux and Initiation à la programmation C)
  • After the thesis: decision process still in progress :(){ :|:& };:
PUBLICATIONS & PATENTS

• Short papers :
  • Julien Rodriguez, Evaluation of the potential of quantum computing for combinatorial optimization, Conférence pour la Recherche opérationnelle et aide à la décision en France, 2021 (Finalist for the Master's thesis award)
  • Julien Rodriguez and al. Circuit partitioning with delay-based minimization, 31st European Conference on Operational Research, 2021

• School :
  • GDR RO/IA : The international autumn school on Constraint Programming, Combinatorial Optimization and Machine Learning (2020)
References

1. https://www.cea.fr/cea-tech/leti/Documents/d%C3%A9monstrateurs/Flyer_DNEURO.pdf
3. https://deephealth-project.eu
7. Jun 'ichiro MINAMI, Tetsushi KOIDE, Shin'ichi WAKABAYASHI, A Circuit Partitioning Algorithm under Path Delay Constraints (Hiroshima University), 1998
8. Shih-Lian Ou and Massoud Pedram, Timing-driven Placement Based on Partitioning with Dynamic Cut-net Control (University of Southern California) 2000
9. Cristinel Ababei, Navaratnasingh Selvakumaran, Kia Bazargan, George Karypis, Multi-objective Circuit Partitioning for Cutsize and Path-Based Delay Minimization (University of Minnesota) 2002
10. Sin-Hong Liou, Sean Liu, Richard Sun and Hung-Ming Chen Timing Driven Partition for Multi-FPGA Systems with TDM Awareness (University Hsinchu and Synopsys) 2020